INFORMATION DISCLOSURE STATEMENT

Applicants:	Kianian et al.
Application No.	09/982,413
Filed:	October 17, 2001
For:	Semiconductor Memory Array Of Floating Gate Memory Cells With Buried Bit Line & Vertical Word Line Transistor
Group Art Unit:	2826
Examiner:	Scott R. Wilson
Attorney Docket No.:	2102397-992010

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. § 1.56(a) and 37 C.F.R. § 1.97, Applicant(s) hereby make of record the references listed on the accompanying Form PTO-1449 for consideration by the Examiner in connection with the examination of the above-identified patent application.

This Information Disclosure Statement:

(a) ☒ accompanies an RCE patent application submitted herewith.

(b) ☐ is filed within three (3) months of the Filing Date or before the mailing date of a First Office Action on the merits; **OR**

(c) ☐ is filed after the first Office Action and more than three months after the application's filing date or PCT national stage date of entry filing but, as far as is known to the undersigned prior to the mailing date of either a final rejection or a notice of allowance, and is accompanied by either the fee ($180) set forth in 37 CFR § 1.17(p) or a certification as specified in 37 CFR § 1.97(e), as checked below **OR**

(d) ☐ is filed after the mailing date of either a final rejection or a notice of allowance, and the issue fee has not been paid, and is accompanied by the requisite petition fee ($130) set forth in 37 CFR § 1.17(l)(1) and a certification as specified in 37 CFR § 1.97(e), as checked below. This document is to be considered as a petition requesting consideration of the information disclosure statement.

As required under § 1.97(e), Applicants, through the undersigned, hereby state either that [check the appropriate space]:

(e) ☐ Each item of information contained in the Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing date of the Information Disclosure Statement; or

(f) ☐ No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this Statement after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to any individual designated in § 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

It is respectfully requested that each of the references shown on the attached Form PTO-1449 be made of record in this application. Copies of the references are enclosed

The Commissioner is authorized to charge any deficiencies and credit any overpayment of fees to our Deposit Account No. 07-1896.

Respectfully submitted,

Date: October 8, 2004

GRAY CARY WARE & FREIDENRICH LLP

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as FIRST CLASS MAIL in an envelope addressed to: Commissioner for Patents; P. O. Box 1450, Alexandria, VA 22313-1450.

October 8, 2004
Date

Signature

Form PTO-1449 (modified 2/91) DEPT. OF COMMERCE Patent and Trademark Office **INFORMATION DISCLOSURE CITATION** (Use several sheets if necessary)	Attorney Docket Number: 2102397-992010	Serial Number: 09/982,413
	Applicants: Kianian et al.	
	Filing date: October 17, 2001	Group art unit: 2826

U.S. PATENT DOCUMENTS

Examiner Initial	Patent No. Publication No.	Date	Name	Class	Sub-class	Filing date if appropriate
	5,338,953	08/1994	Wake			
	5,943,572	08/1999	Krautschneider			
	6,180,458	01/2001	Krautschneider et al.			
	6,538,275	03/2003	Sugiyama, et al.			
	6,541,815	04/2003	Mandelman, et al.			
	6,756,633	06/2004	Wang et al.			
	10/776,483	02/2004	Kianian et al.			
	10/105,741	03/2002	Kianian			
	10/653,015	08/2003	Chen et al.			
	10/776,397	02/2004	Kianian et al.			
	10/818,590	04/2004	Kianian et al.			

FOREIGN PATENT DOCUMENTS

	Document number	Date	Country	Class	Sub-class	Translation YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	SZE, Simon, "Physics of Semiconductor Devices", 2nd Edition, Wiley-Interscience, Basic Device Characteristics, pages 438-439.
	BROWN, William D., et al..; "Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide To Understanding And Using NVSM Devices", IEEE Press, pages 33-34.
	HAYASHI, et al., "A Self-aligned Split-Gate Flash EEPROM Cell With 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pp. 87-88, Center for Integrated Systems, Stanford University, Stanford, CA 94305, USA.

Examiner:	Date Considered:
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP '609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.	